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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Phadnis et al

Appl. No.: 09/976,004

Filed: October 15, 2001

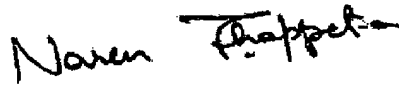
For: Reducing Overhead When Setting Up Multiple
Virtual Circuits Using Signaling Protocols

Art Unit: 2661

Examiner: Robert W. Wilson

Atty. Docket: CSCO-010/4390

I hereby certify that this correspondence is being facsimile
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2006



(Signature)

By: Narendra R. Thappeta (Type Name)

TRANSMITTAL LETTER

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In connection with the above-referenced U. S. patent application, transmitted herewith are
the following papers:

- [x] This Cover Letter (2 Pages in duplicate);
- [x] Petition for extension of time under 37 CFR § 1.136(a) (1 Page);
- [x] Credit Card Authorization Payment Form for \$120.00 to cover the one-month extension of
time under 37 CFR § 1.136(a) (1 Page); and
- [x] Amendment and Response Under 37 C.F.R. §§ 1.111 (18 Pages).

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